

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Jin-Koo Rhee et al.

Serial No:

09/755,436

Filed:

January 4, 2001

For:

TRANSISTOR WITH # GATE

STRUCTURE AND METHOD FOR

PRODUCING THE SAME

<u>AMENDMENT</u>

Box Non-Fee Assistant Commissioner for Patents Washington, D.C. 20231 Art Unit:

2827

Examiner:

Luan C. Thai

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Assistant Commissioner for Patents Washington D.C. 20231, on January 2, 2003

Date of Deposit

Amit Sheth Name

Signature

01/ *2* /03 Date

Dear Sir:

In response to the Office Action dated October 4, 2002, in connection with the above-identified application, please enter and consider the following amendments and remarks:

IN THE ABSTRACT:

Please substitute the abstract of the disclosure originally filed with the present application with the substitute abstract attached hereto.

IN THE CLAIMS:

Please amend claim 1 and add new claims 3-6 as follows:

Please substitute the claims listed below for the pending claims with the same number:

Marked-Up Claim:

1. (Amended) A transistor [with π – gate structure, with a GaAs wafer formed on the bottom with GND, which is grounded to source layers formed on the top surface of the GaAs wafer by the process of back side via-hole, with a drain formed between the source layers, the top part of which has an air-layer, and with a gate shaped, as the result of using the air bridge